

# PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2001-309642

(43)Date of publication of application : 02.11.2001

(51)Int.Cl.

H02M 3/07

(21)Application number : 2000-125094

(71)Applicant : NEW JAPAN RADIO CO LTD

(22)Date of filing : 26.04.2000

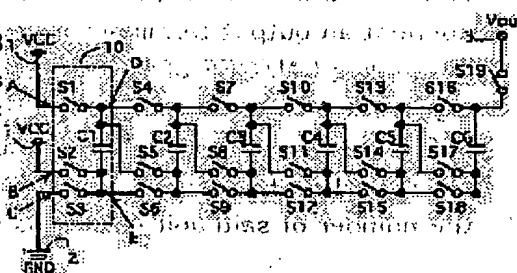
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## (54) VARIABLE BOOSTING CIRCUIT

### (57)Abstract:

**PROBLEM TO BE SOLVED:** To materialize a variable boosting circuit and reducing the number of switches for use in an output terminal.

**SOLUTION:** A unit circuit 10 is composed of a condenser C1 and switches S1, S2 and S3. Two or more unit circuits are cascade-connected by connecting nodes A, B of another unit circuit to a node D of one unit circuit, and connecting a node E to a node C. The nodes A, B of the first-step circuit is connected to VCC and the node C to GND, as well as the node D of the last-step unit circuit is connected to the output terminal 3 through S19. The unit circuit is cascade-connected in N steps ( $N \geq 2$  of even number) and by switching S1 to S3 of each unit circuit and S19 on-off, one boosting voltage among multiples of  $N+1$ ,  $N/2+1$ , 3 and 2 is selectively output.



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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**CLAIMS**

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[Claim(s)]

[Claim 1] A capacitor and the 1st switch on which the end was connected to the end of this capacitor, A unit circuit is constituted from the 2nd and 3rd switch on which the end was connected to the other end of said capacitor. And the other end of Node D and said capacitor is made [ the other end of said 1st switch / Node A and the other end of said 2nd switch / Node B and the other end of said 3rd switch ] into Node E for the end of Node C and said capacitor. Two or more unit circuits are cascaded by connecting Node C to the node D of a certain unit circuit for the nodes A and B of another unit circuit at Node E. Connect a high potential power supply terminal to the nodes A and B of the unit circuit of the first rank, and a low voltage power supply terminal is connected to Node C. By coming to connect an output terminal with the node D of the unit circuit of a tail end through the 4th switch, and controlling ON/OFF of the 1st, 2nd, and 3rd switch of each unit circuit, and said 4th switch The adjustable booster circuit characterized by making it output alternatively any one electrical potential difference in the twice of the electrical potential difference of said high potential power supply terminal, 3 times,  $N/2+1$  time, and  $N+1$  time which carried out the pressure up from said output terminal when the number of said unit circuits is set to N (two or more even number).

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**DETAILED DESCRIPTION**

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[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the adjustable booster circuit which enabled it to change output voltage.

[0002]

[Description of the Prior Art] This kind of adjustable booster circuit is shown in drawing 7 . As for C51 and C52, a capacitor, and S51-S58 are switches. As for a high potential power-source (VCC) terminal and 2, 1 is [ a low voltage power-source (GND) terminal and 3 ] output terminals. A 3 time pressure up

and 2 double pressure up are possible in this booster circuit.

[0003] (Time [ 3 ] pressure-up actuation: Drawing 8 ) The switch S54 is fixed to OFF at the time of this 3 time pressure up.

[0004] (a) .. Switches S52, S53, S56, and S57 are made to turn on, and switches S51, S55, and S58 are made to turn off.

[0005] (b) .. Switches S52, S53, S56, and S57 are made to turn off, and switches S51, S55, and S58 are made to turn on.

[0006] If each switch is changed as shown in (a), it will become a circuit as shown in (a) of drawing 8 , and supply voltage VCC will be charged by capacitors C51 and C52 with the polarity of illustration. Next, if each switch is changed as shown in (b), it will become a circuit as shown in (b) of drawing 8 , the electrical potential difference of a capacitor C51 and the electrical potential difference of C52 will be added by like-pole nature to the electrical potential difference of a power supply terminal 1, and the electrical potential difference of 3VCC(s) will occur in an output terminal 3. Therefore, the electrical potential difference of stable 3VCC(s) can be taken out from an output terminal 3 by repeating the switch change condition of (a) of drawing 8 , and (b) by turns.

[0007] (2 double pressure-up actuation: Drawing 9 ) Switches S55 and S58 are fixed to OFF at the time of this 2 double pressure up, and it fixes switches S56 and S57 to ON or OFF.

[0008] (a) .. Switches S52 and S53 are turned on and switches S51 and S54 are made to turn off.

[0009] (b) .. Switches S52 and S53 are turned off and switches S51 and S54 are made to turn on.

[0010] If each switch is changed as shown in (a), it will become a circuit as shown in (a) of drawing 9 , and supply voltage VCC will be charged by the capacitor C51 with the polarity of illustration. Next, if each switch is changed as shown in (b), it will become a circuit as shown in (b) of drawing 9 , the electrical potential difference of a capacitor C51 will be added by like-pole nature to the electrical potential difference of a power supply terminal 1, and the electrical potential difference of 2VCC(s) will occur in an output terminal 3. Therefore, the electrical potential difference of stable 2VCC(s) can be taken out from an output terminal 3 by repeating the switch change condition of (a) of drawing 9 , and (b) by turns.

[0011]

[Problem(s) to be Solved by the Invention] However, switches S54 and S58 are needed in this booster circuit for the change of the capacitors C51 and C52 linked to an output terminal 3. When making a booster circuit in a semiconductor integrated circuit, since size becomes large compared with transistors, such as a logic gate, the transistor which functions as a switch will cause chip area increase, if the number of switches increases. Moreover, in the time of 2 double pressure up, one capacitor C51 does not contribute to a pressure up, but the use effectiveness of a capacitor is bad.

[0012] The purpose of this invention is offering the adjustable booster circuit which made pressure-up effectiveness high as suppressed chip area increase as the switch which changes the capacitor linked to an output terminal was unnecessary, and could contribute all capacitors to pressure-up actuation.

[0013]

[Means for Solving the Problem] The 1st switch by which, as for this invention for solving the above-mentioned technical problem, the end was connected to the end of a capacitor and this capacitor, A unit circuit is constituted from the 2nd and 3rd switch on which the end was connected to the other end of said capacitor. And the other end of Node D and said capacitor is made [ the other end of said 1st switch / Node A and the other end of said 2nd switch / Node B and the other end of said 3rd switch ] into Node E for the end of Node C and said capacitor. Two or more unit circuits are cascaded by connecting Node C to the node D of a certain unit circuit for the nodes A and B of another unit circuit at Node E. Connect a high potential power supply terminal to the nodes A and B of the unit circuit of the first rank, and a low voltage power supply terminal is connected to Node C. By coming to connect an output terminal with the node D of the unit circuit of a tail end through the 4th switch, and controlling ON/OFF of the 1st, 2nd, and 3rd switch of each unit circuit, and said 4th switch When the number of

said unit circuits was set to N (two or more even number), it was made to output alternatively any one electrical potential difference in the twice of the electrical potential difference of said high potential power supply terminal, 3 times,  $N / 2 + 1$  time, and  $N + 1$  time which carried out the pressure up from said output terminal.

[0014]

[Embodiment of the Invention] [Gestalt of the 1st operation] drawing 1 is the circuit diagram of the adjustable booster circuit of the gestalt of operation of the 1st of this invention. For a capacitor, and S1–S19, as for a high potential power-source (VCC) terminal and 2, a switch and 1 are [ C1–C6 / a low voltage power-source (GND) terminal and 3 ] output terminals. 10 is a unit circuit which consists of a capacitor C1 and switches S1–S3, and this adjustable booster circuit carries out six-step cascade connection (cascade connection) of this unit circuit 10. The nodes A and B were connected to the power supply terminal 1, and it connected Node C to the low voltage power supply terminal 2 respectively, and the unit circuit 10 of the first rank connects Node D to the nodes A and B of the unit circuit of the next step, and has connected Node E to the node C of the unit circuit of the next step. Moreover, the unit circuit of a tail end has connected the node D to an output terminal 3 through a switch S19.

[0015] A 7 times, 4 times, 3 times, and twice as many pressure up as this is possible by the change of switches S1–S19 in this booster circuit.

[0016] (Time [ 7 ] pressure-up actuation: Drawing 2 and drawing 3 )

(a) .. Switches S1 and S3, S4, S6 and S7, S9, and S10, S12, S13, S15, S16 and S18 are made to turn on, and the remaining switch is made to turn off. By this, as shown in drawing 2 , supply voltage VCC is separately charged by each capacitors C1–C6.

[0017] (b) .. Each switch is changed to the above and reverse. As shown in drawing 3 , the series connection of the capacitors C1–C6 is carried out between a power supply terminal 1 and an output terminal 3 by this, and the electrical potential difference of  $7VCC(s)$  by which the electrical potential difference VCC of a power supply terminal 1 was added to the electrical potential difference VCC of each capacitors C1–C6 by like-pole nature appears in an output terminal 3.

[0018] Therefore, the electrical potential difference of a pressure up is obtained 7 times stabilized in the output terminal 3 by changing the switch condition of drawing 2 , and the switch condition of drawing 3 by turns.

[0019] (Time [ 4 ] pressure-up actuation: Drawing 2 and drawing 4 )

(c) .. After changing to the condition of drawing 2 , a switch S2, S4, and S6, S8, S10, S12, S14, S16, S18 and S19 are made to turn on, and the remainder is turned OFF. As this shows to drawing 4 , parallel connection of C4, C5, and C6 is respectively carried out to a capacitor C1, and C2 and C3, and series connection of these is carried out between a power supply terminal 1 and an output terminal 3, and the electrical potential difference of  $4VCC$  appears in an output terminal 3.

[0020] Therefore, the electrical potential difference of a pressure up is obtained 4 times stabilized in the output terminal 3 by changing the switch condition of drawing 2 , and the switch condition of drawing 4 by turns. Since parallel connection of each two capacitors C1–C6 of every is carried out at this time, that pressure-up capacity becomes large and a big load can be borne.

[0021] (Time [ 3 ] pressure-up actuation: Drawing 2 and drawing 5 )

(d) .. After changing to the condition of drawing 2 , a switch S2, S4, S6 and S7, S9, and S11, S13, S15, S16, S18 and S19 are made to turn on, and the remainder is turned OFF. As this shows to drawing 5 , parallel connection of C5 and C6 is respectively carried out to capacitors C1 and C2, and C3 and C4, and series connection of these is carried out between a power supply terminal 1 and an output terminal 3, and the electrical potential difference of  $3VCC$  appears in an output terminal 3.

[0022] Therefore, the electrical potential difference of a pressure up is obtained 3 times stabilized in the output terminal 3 by changing the switch condition of drawing 2 , and the switch condition of drawing 5 by turns. Since parallel connection of each three capacitors C1–C6 of every is carried out at this time,

that pressure-up capacity becomes large and a big load can be borne. [0023] (2 double pressure-up actuation: Drawing 2 and drawing 6 ) (e) . After changing to the condition of drawing 2 , a switch S2, S4, S6 and S7, S9, and S10, S12, S13, S15, S16, S18 and S19 are made to turn on, and the remainder is turned OFF. As this shows to drawing 6 , parallel connection of the capacitors C1-C6 is carried out, and series connection of these is carried out by like-pole nature between a power supply terminal 1 and an output terminal 3, and the electrical potential difference of 2VCC appears in an output terminal 3. [0024] Therefore, the electrical potential difference of 2 double pressure up stabilized in the output terminal 3 is obtained by changing the switch condition of drawing 2 , and the switch condition of drawing 6 by turns. Since parallel connection of those all is carried out at this time, that pressure-up capacity becomes large and each capacitors C1-C6 can bear a big load. [0025] In addition, although six steps of unit circuits 10 were cascaded and 7 times, 4 times, 3 times, and 2 double pressure up were realized above, if it is made eight steps, and 9 times, 5 times, 3 times, and 2 double pressure up make it ten steps, 11 times, 6 times, 3 times, and 2 double pressure up of them will become possible. That is, an N+1 time, N / 2+1 time, 3 times, and twice as many adjustable pressure up as this is realizable in this unit circuit by carrying out N stage (two or more even number) cascade connection of the unit circuit.

[0026]

[Effect of the Invention] As mentioned above, according to this invention, the switch which connects a capacitor to an output terminal can be managed with one piece. Moreover, by carrying out N stage (two or more even number) cascade connection of the unit circuit, an N+1 time, N / 2+1 time, 3 times, and twice as many adjustable pressure up as this can be realized, and it becomes usable at a wide range application. Furthermore, since pressure-up actuation can be presented with the capacitor of each stage without futility, pressure-up power also becomes large.

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#### DESCRIPTION OF DRAWINGS

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##### [Brief Description of the Drawings]

[Drawing 1] It is the circuit diagram of the booster circuit of the 1st operation gestalt.

[Drawing 2] It is the explanatory view of the charge to each capacitor of the circuit of drawing 1 .

[Drawing 3] It is the explanatory view of the 7 time pressure up of the circuit of drawing 1 .

[Drawing 4] It is the explanatory view of the 4 time pressure up of the circuit of drawing 1 .

[Drawing 5] It is the explanatory view of the 3 time pressure up of the circuit of drawing 1 .

[Drawing 6] It is the explanatory view of 2 double pressure up of the circuit of drawing 1 .

[Drawing 7] It is the circuit diagram of the conventional booster circuit.

[Drawing 8] It is the explanatory view of the 3 time pressure up of the circuit of drawing 7 .

[Drawing 9] It is the explanatory view of 2 double pressure up of the circuit of drawing 7 :

[Description of Notations]

10: Unit circuit

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(19)日本国特許庁(JP)

(12) 公開特許公報 (A)

(11)特許出願公開番号

特開2001-309642

(P2001-309642A)

(43)公開日 平成13年11月2日(2001.11.2)

(51)Int.Cl.<sup>7</sup>

H02M 3/07

識別記号

FI

H02M 3/07

テ-マ-ト(参考)

5H730

審査請求 未請求 請求項の数1 OL (全5頁)

(21)出願番号 特願2000-125094(P2000-125094)

(22)出願日 平成12年4月26日(2000.4.26)

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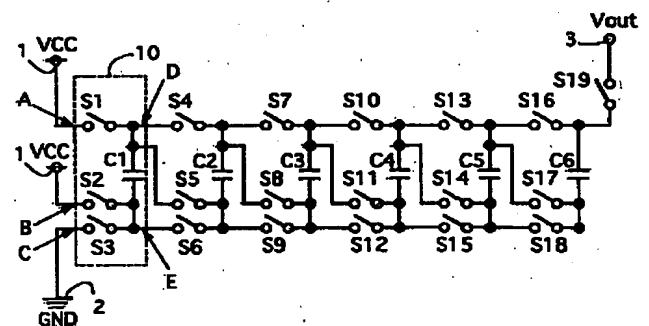
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(54)【発明の名称】 可変昇圧回路

(57)【要約】

【課題】 可変昇圧回路を実現し、出力端子に対するスイッチ数を削減する。

【解決手段】 コンデンサC1、スイッチS1、S2、S3から単位回路10を構成する。ある単位回路のノードDに別の単位回路のノードA、Bを、ノードCにノードEを接続することにより2以上の単位回路を縦属接続する。初段の単位回路のノードA、BにVCCを、ノードCにGNDを接続すると共に終段の単位回路のノードDにS19を介して出力端子3を接続する。単位回路をN段( $N \geq 2$ の偶数)縦属接続し、各単位回路のS1~S3、S19をオン/オフすることにより、 $N+1$ 倍、 $N/2+1$ 倍、3倍、2倍のうちのいずれか1つの昇圧電圧を選択的に出力する。



(2)

1

## 【特許請求の範囲】

【請求項1】コンデンサと、該コンデンサの一端に一端が接続された第1のスイッチと、前記コンデンサの他端に一端が接続された第2、第3のスイッチとから単位回路を構成し、且つ前記第1のスイッチの他端をノードA、前記第2のスイッチの他端をノードB、前記第3のスイッチの他端をノードC、前記コンデンサの一端をノードD、前記コンデンサの他端をノードEとして、ある単位回路のノードDに別の単位回路のノードA、Bを、ノードEにノードCを接続することにより2以上の単位回路を縦属接続して、初段の単位回路のノードA、Bに高電位電源端子を接続し、ノードCに低電位電源端子を接続し、終段の単位回路のノードDに第4のスイッチを介して出力端子を接続してなり、各単位回路の第1、第2、第3のスイッチ及び前記第4のスイッチのオン/オフを制御することにより、前記単位回路の数をN（2以上の偶数）としたとき、前記出力端子から前記高電位電源端子の電圧の2倍、3倍、 $N/2 + 1$ 倍、 $N + 1$ 倍のうちのいずれか1つの昇圧した電圧を選択的に出力するようにしたことを特徴とする可変昇圧回路。

## 【発明の詳細な説明】

## 【0001】

【発明の属する技術分野】本発明は、出力電圧を切り替えることができるようにした可変昇圧回路に関するものである。

## 【0002】

【従来の技術】図7にこの種の可変昇圧回路を示す。C51、C52はコンデンサ、S51～S58はスイッチである。1は高電位電源（VCC）端子、2は低電位電源（GND）端子、3は出力端子である。本昇圧回路では、3倍昇圧と2倍昇圧が可能である。

【0003】（3倍昇圧動作：図8）この3倍昇圧のときは、スイッチS54はオフに固定しておく。

【0004】(a)・・・スイッチS52、S53、S56、S57をオンさせ、スイッチS51、S55、S58をオフさせる。

【0005】(b)・・・スイッチS52、S53、S56、S57をオフさせ、スイッチS51、S55、S58をオンさせる。

【0006】(a)のように各スイッチを切り替えると、図8の(a)に示すような回路となり、コンデンサC51、C52に電源電圧VCCが図示の極性で充電される。次に(b)に示すように各スイッチを切り替えると、図8の(b)に示すような回路となり、電源端子1の電圧に対してコンデンサC51の電圧とC52の電圧が同極性で加算されて、出力端子3に3VCCの電圧が発生する。したがって、図8の(a)と(b)のスイッチ切替状態を交互に繰り返すことによって、安定した3VCCの電圧を出力端子3から取り出すことができる。

2

【0007】（2倍昇圧動作：図9）この2倍昇圧のときは、スイッチS55、S58をオフに固定し、スイッチS56、S57をオン又はオフに固定しておく。

【0008】(a)・・・スイッチS52、S53をオンし、スイッチS51、S54をオフさせる。

【0009】(b)・・・スイッチS52、S53をオフし、スイッチS51、S54をオンさせる。

【0010】(a)のように各スイッチを切り替えると、図9の(a)に示すような回路となり、コンデンサC51に電源電圧VCCが図示の極性で充電される。次に(b)に示すように各スイッチを切り替えると、図9の(b)に示すような回路となり、電源端子1の電圧に対してコンデンサC51の電圧が同極性で加算されて、出力端子3に2VCCの電圧が発生する。したがって、図9の(a)と(b)のスイッチ切替状態を交互に繰り返すことによって、安定した2VCCの電圧を出力端子3から取り出すことができる。

## 【0011】

【発明が解決しようとする課題】ところが、この昇圧回路では、出力端子3に接続するコンデンサC51、C52の切替用にスイッチS54、S58が必要となっている。昇圧回路を半導体集積回路内に作り込む場合、スイッチとして機能するトランジスタは論理ゲート等のトランジスタに比べてサイズが大きくなるので、スイッチ数が増大するとチップ面積増大を招く。また、2倍昇圧時では1個のコンデンサC51が昇圧に寄与しておらず、コンデンサの利用効率が悪い。

【0012】本発明の目的は、出力端子に接続するコンデンサを切り替えるスイッチが必要ないようにして、チップ面積増大を抑え、また昇圧動作に全部のコンデンサが寄与できるようにして昇圧効率を高くした可変昇圧回路を提供することである。

## 【0013】

【課題を解決するための手段】上記課題を解決するための本発明は、コンデンサと、該コンデンサの一端に一端が接続された第1のスイッチと、前記コンデンサの他端に一端が接続された第2、第3のスイッチとから単位回路を構成し、且つ前記第1のスイッチの他端をノードA、前記第2のスイッチの他端をノードB、前記第3のスイッチの他端をノードC、前記コンデンサの一端をノードD、前記コンデンサの他端をノードEとして、ある単位回路のノードDに別の単位回路のノードA、Bを、ノードEにノードCを接続することにより2以上の単位回路を縦属接続して、初段の単位回路のノードA、Bに高電位電源端子を接続し、ノードCに低電位電源端子を接続し、終段の単位回路のノードDに第4のスイッチを介して出力端子を接続してなり、各単位回路の第1、第2、第3のスイッチ及び前記第4のスイッチのオン/オフを制御することにより、前記単位回路の数をN（2以上の偶数）としたとき、前記出力端子から前記高電位電



(3)

3

源端子の電圧の2倍、3倍、 $N/2+1$ 倍、 $N+1$ 倍のうちのいずれか1つの昇圧した電圧を選択的に出力するようにした。

【0014】

【発明の実施の形態】【第1の実施の形態】図1は本発明の第1の実施の形態の可変昇圧回路の回路図である。C1～C6はコンデンサ、S1～S19はスイッチ、1は高電位電源(VCC)端子、2は低電位電源(GND)端子、3は出力端子である。10はコンデンサC1、スイッチS1～S3よりなる単位回路であり、本可変昇圧回路はこの単位回路10を6段縦属接続(カスケード接続)したものである。初段の単位回路10はそのノードA、Bを電源端子1に、ノードCを低電位電源端子2に各々接続し、ノードDを次段の単位回路のノードA、Bに、ノードEを次段の単位回路のノードCに接続している。また、終段の単位回路はそのノードDをスイッチS19を介して出力端子3に接続している。

【0015】本昇圧回路では、スイッチS1～S19の切り替えによって、7倍、4倍、3倍、2倍の昇圧が可能である。

【0016】(7倍昇圧動作：図2と図3)

(a)・・・スイッチS1、S3、S4、S6、S7、S9、S10、S12、S13、S15、S16、S18をオンさせ、残りのスイッチをオフさせる。これによって、図2に示すように各コンデンサC1～C6に個々に電源電圧VCCが充電される。

【0017】(b)・・・各スイッチを上記と逆に切り替える。これによって、図3に示すようにコンデンサC1～C6が電源端子1と出力端子3の間に直列接続され、各コンデンサC1～C6の電圧VCCに電源端子1の電圧VCCが同極性で加算された7VCCの電圧が出力端子3に現れる。

【0018】よって、図2のスイッチ状態と図3のスイッチ状態を交互に切り替えることによって、出力端子3に安定した7倍昇圧の電圧が得られる。

【0019】(4倍昇圧動作：図2と図4)

(c)・・・図2の状態に切り替えた後、スイッチS2、S4、S6、S8、S10、S12、S14、S16、S18、S19をオンさせ残りをオフにする。これによって図4に示すようにコンデンサC1とC2、C3とC4、C5とC6が各々並列接続され且つこれらが電源端子1と出力端子3の間に直列接続され、4VCCの電圧が出力端子3に現れる。

【0020】よって、図2のスイッチ状態と図4のスイッチ状態を交互に切り替えることによって、出力端子3に安定した4倍昇圧の電圧が得られる。このとき、各コンデンサC1～C6は2個ずつ並列接続されるので、その昇圧容量が大きくなり、大きな負荷に耐えることができる。

【0021】(3倍昇圧動作：図2と図5)

4

(d)・・・図2の状態に切り替えた後、スイッチS2、S4、S6、S7、S9、S11、S13、S15、S16、S18、S19をオンさせ残りをオフにする。これによって図5に示すようにコンデンサC1とC2とC3、C4とC5とC6が各々並列接続され且つこれらが電源端子1と出力端子3の間に直列接続され、3VCCの電圧が出力端子3に現れる。

【0022】よって、図2のスイッチ状態と図5のスイッチ状態を交互に切り替えることによって、出力端子3に安定した3倍昇圧の電圧が得られる。このとき、各コンデンサC1～C6は3個ずつ並列接続されるので、その昇圧容量が大きくなり、大きな負荷に耐えることができる。

【0023】(2倍昇圧動作：図2と図6)

(e)・・・図2の状態に切り替えた後、スイッチS2、S4、S6、S7、S9、S10、S12、S13、S15、S16、S18、S19をオンさせ残りをオフにする。これによって図6に示すようにコンデンサC1～C6が並列接続され且つこれらが電源端子1と出力端子3の間に同極性で直列接続され、2VCCの電圧が出力端子3に現れる。

【0024】よって、図2のスイッチ状態と図6のスイッチ状態を交互に切り替えることによって、出力端子3に安定した2倍昇圧の電圧が得られる。このとき、各コンデンサC1～C6はその全部が並列接続されるので、その昇圧容量が大きくなり、大きな負荷に耐えることができる。

【0025】なお、以上では単位回路10を6段縦属接続して、7倍、4倍、3倍、2倍昇圧を実現したが、8段にすると9倍、5倍、3倍、2倍昇圧が、10段にすると11倍、6倍、3倍、2倍昇圧が可能となる。つまり、この単位回路では、単位回路をN段(2以上の偶数)縦属接続することにより、 $N+1$ 倍、 $N/2+1$ 倍、3倍、2倍の可変昇圧が実現できる。

【0026】

【発明の効果】以上から本発明によれば、コンデンサを出力端子に対して接続するスイッチは1個で済む。また、単位回路をN段(2以上の偶数)縦属接続することにより、 $N+1$ 倍、 $N/2+1$ 倍、3倍、2倍の可変昇圧が実現でき、広範囲の用途に使用可能となる。さらに、各段のコンデンサを無駄なく昇圧動作に供することができるので、昇圧電力も大きくなる。

【図面の簡単な説明】

【図1】は第1の実施形態の昇圧回路の回路図である。

【図2】は図1の回路の各コンデンサへの充電の説明図である。

【図3】は図1の回路の7倍昇圧の説明図である。

【図4】は図1の回路の4倍昇圧の説明図である。

【図5】は図1の回路の3倍昇圧の説明図である。

【図6】は図1の回路の2倍昇圧の説明図である。

(4)

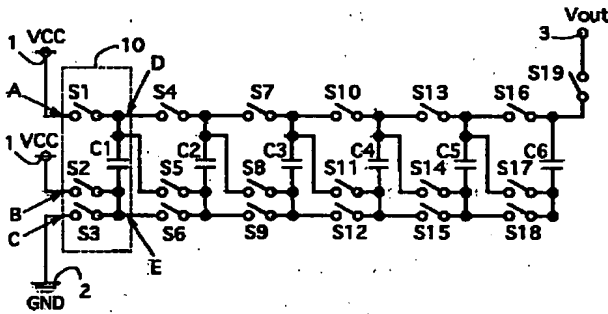
5

【図7】 従来の昇圧回路の回路図である。

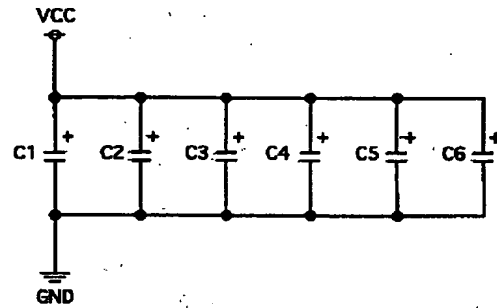
【図8】 図7の回路の3倍昇圧の説明図である。

【図9】 図7の回路の2倍昇圧の説明図である。

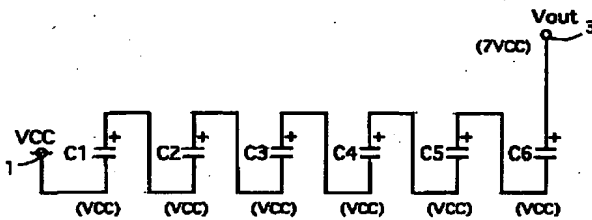
【図1】



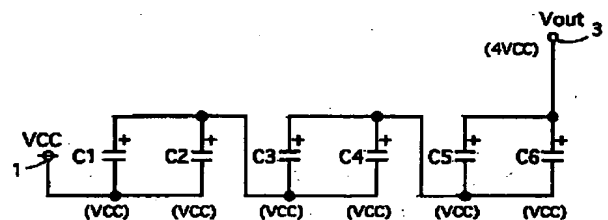
【図2】



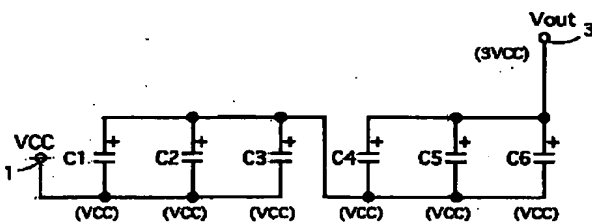
【図3】



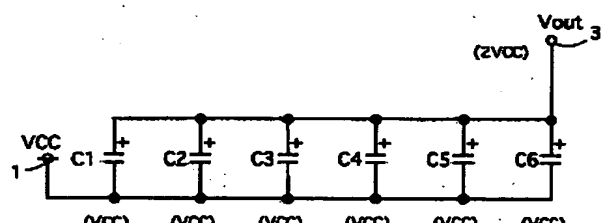
【図4】



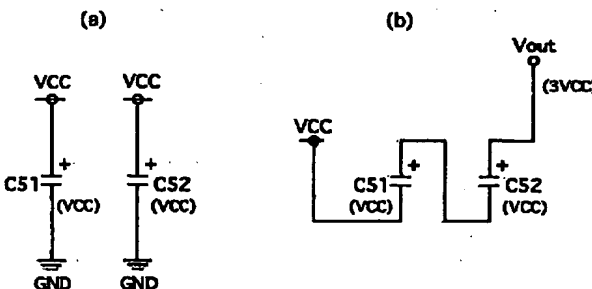
【図5】



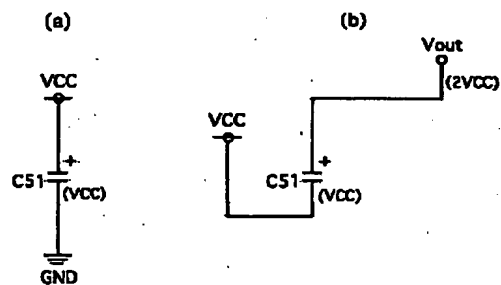
【図6】



【図8】

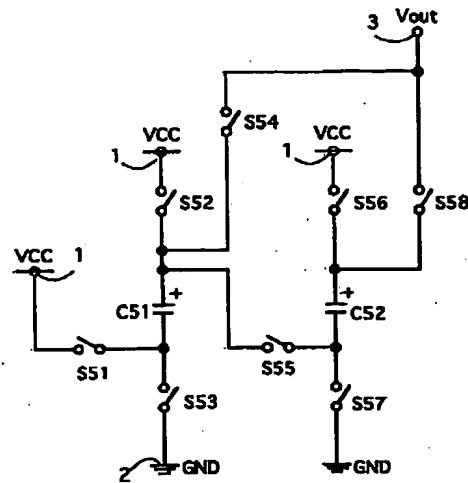


【図9】



(5)

【図7】



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フロントページの続き

Fターム(参考) 5H730 AA11 AA16 AS04 BB02 BB57  
BB86 BB88 BB89 BB98 DD01  
DD12 DD26 DD32 FD01 FG01  
FG16 FG22